REMARKS

This Amendment is filed in response to the FINAL Office Action mailed on November 23, 2005. All objections and rejections are respectfully traversed.

Claims 67-117 are in the case.

Claims 67, 84, 92, 111, 117 were amended to correct a spelling error.

No claims were added.

At Paragraphs 3-4 Claim 117 was rejected under 35 U.S.C. 112, first paragraph.

The present invention, as set forth by representative claim 117, comprises in part:

117. A computer readable media, comprising: the computer read-able media containing instructions for execution in a processor for the practice of the method of,
providing a multiplexer (MUX) having a first and second MUX in-put and a MUX output;
coupling the first MUX input to a first input of a first ALU;
coupling a second MUX input to a first input register of a second ALU; and
directly providing, by the MUX output, a first input to the second ALU, the MUX permitting both the first and second ALU to share a source operand stored in a first input register of the first ALU.

At paragraphs 8-9A the Examiner replied to Applicant's arguments filed on September 6, 2005.

The Examiner states:

"Applicant has now placed of record within the application history an explicit statement that claim 117 is both inherent to any computer programmer, and is obvious to anyone of skill in the relevant art. Applicant's statement indicates that the claim can never be allowed."

Applicant respectfully points out that the Examiner is wrong in this statement. Apparently the Examiner misunderstands Applicant's argument, which is quoted by the Examiner as:

"The computer readable media claim makes a knock off artist a direct infringer. Furthermore, the computer readable media claim includes preventing downloading a file from a web site. Downloading a file is inherent knowledge of every computer programmer. That is anyone that can design the invention under claims 67, 84, 92, or 111 has the ordinary skill in the art to design the invention under claim 117."

This argument plainly states that the novel invention, as set forth in representative claims 67, 84, 92, and 111 is novel and patentable. Once a person of ordinary skill in the art of computer design is taught the presently claimed invention, by, for example, reading the Specification of the present patent application, that person of ordinary skill can write his computer program to a computer readable media, as claimed in Claim 117.

Accordingly, Claim 117 meets all requirements of 35 U.S.C. 112, first paragraph. That is, a person of ordinary skill in the art is enabled by the Specification to make and use the claimed invention, without having to go through undue experimentation.

At Paragraphs 5, 7, 8, and 9B of the Office Action Claims 67-72, 78-97, and 104-117 were rejected under 35 U.S.C. 102(b) as being anticipated by Hao, et al. U. S. Patent No. 4,594,665 issued June 10, 1986 (hereinafter Hao).

The present invention, as set forth in representative claim 67, comprises in part:

67. A processor, comprising:

a first execution unit having a first and second input register coupled to first and second inputs to a first arithmetic logic unit (ALU), the first and second input registers of the first execution unit to store source operands;

a second execution unit having a first and second input register, the second register coupled to a second input to a second ALU, the first and second input registers of the second execution unit to store source operands; and

a multiplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.

The Examiner, at Paragraph 9B of the Office Action, argues that Applicant's argument filed September 6, 2005, at Page 15 last paragraph is not persuasive. Applicant's Argument is set out as:

"The geometry in Hao does not disclose the use of a ***Multiplexer***. In paragraph 8(D) of the Office Action, the Examiner states that element 22 in Figure 1 is a multiplexer. However, at Col. 6, line 8, the specification states "three-input binary adder 22." Furthermore, in the figures and detailed description of Hao, there is no description of using a ***multiplexer*** as described in Applicant's invention. Hao is silent describing using a multiplexer to select inputs for an ALU, as claimed by applicant."

(Applicant's argument filed September 6, 2005, at Page 15 last paragraph.)

The Examiner further argues:

"This is not found persuasive because had applicant read the entire citation, and not just the last two words, he would have found this statement:

"mux shown just above the letter A at element 22"

Element 22 was not being referenced as the mux, but was being referenced as a relative location point to allow applicant to locate the mux. Furthermore, Hao explicitly details multiplexers at col. 6 lines 29-35:

> The secondary execution unit (left portion of FIG. 1) comprises a limited set of functional organs, including ... input multiplexers ..."

Accordingly, Hao does indeed both show in the drawings and discloses in the text a mux, contrary to applicant's arguments."

(Office Action of 11/23/2005 at Paragraph 9B)

Hao at Col. 6 lines 29-35 states:

"The secondary execution unit (left portion of FIG. 1) comprises a limited set of functional organs, including a second set of general purpose registers 24, three-input adder 22, additional ports to and from general purpose registers 24, input multiplexers and input staging registers 25-26, and output staging register 23. The secondary execution unit enables the pipelined processor to process an additional instruction, in addition to the primary instruction undergoing execution in the "conventional facilities" of the primary execution unit. Certain logical interlocks presented by the first instruction may be circumvented by the action of the secondary execution unit, as determined and controlled by the control mechanism."

Operation of the design of Fig. 1 of Hao appears to use the output of register 5 and register 6 to control the switches indicated as "A", "B", and "C" of Hao's ALU 2 "22", and therefore for registers 5 and 6 of ALU 1 to control the inputs to ALU 2. (Note, Hao's reference numerals are enclosed in quote symbols " . . . " in order to distinguish them.)

By the horizontal line from register 5 output, input to ALU 2 at both input "A" from register 25 and input to input "B" from register 26 may be controlled by register 5.

By the lower horizontal line from register 6 output to the input "C" of ALU 2 "22", control is indicated, but there is no signal input line to input "C". Therefore, the best guess is that input "C" of ALU 2 "22" simply disables ALU 2 "22", as described by Hao at his Col. 9 lines 61 through Col. 10 line 4) which state in relevant part:

"As the STAGING CYCLE begins, controls call for "Access source regs for OP1" which accesses OP1 information from GPR's 4 in FIG. 1. Data is set into the staging registers S1 and S2 (5,6 in Fig. 1). In the appropriate situation (a Store instruction) store data is accessed from GPR's 24 (FIG. 1) for the secondary data flow. . . .

The two instructions may be inherently independent, may be inherently sequential but susceptible to parallel execution by the pipelined processor, or may be subject to interlocks which require serial processing"

(Hao Col 9 line 66 – Col. 10 Line 14)

Hao, in the above quoted section, makes a clear assertion that input data for ALU 1 "2" comes from registers 5 and 6, and that input for ALU 2 "22" comes from registers 25 and 26.

Nowhere does Hao even hint that one of his registers 5, 6, 25, and 26 can supply input to both ALU 1 "2" and supply input to ALU 2 "22".

Applicant claims ***a multiplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the sec-***

ond ALU, and iii) an output directly providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.

Applicant's claimed novel use of a multiplexer having ***a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU*** describes a geometric arrangement which permits the ***first input of the first ALU*** to be coupled into the first input of the second ALU. Then, as Applicant further claims, ***the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.***

Applicant respectfully urges that Hao has no disclosure of Applicant's claimed novel, ***the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.***

In sharp contrast, Hao discloses registers 5 and 6 supplying input to his ALU 1 "2", and his registers 25 and 26 supplying input to his ALU 2 "22". Nowhere does Hao have any disclosure of one register providing input to both ALUs, as claimed by Applicant.

Accordingly, Applicant respectfully urges that Hao is legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 102 because of the ab-

sence from Hao of Applicant's claimed novel ***a multiplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.***

At Paragraph 6 of the Office Action Claims 73-77 and 98-103 were rejected under 35 U.S.C. 103 as being unpatentable over Hao in view of Asato U. S. Patent No. 6,145,074 issued November 7, 2000 (hereinafter Asato).

Applicant respectfully points out that Claims 73-77 and 98-103 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

All independent claims are believed to be in condition for allowance.

All dependent claims are dependent from independent claims which are believed to be in condition for allowance. Accordingly, all dependent claims are believed to be in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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